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Fabrication and electrical performance of high-density arrays of nanometric silicon tips

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ABSTRACT

We propose and demonstrate a simple and low cost process for the fabrication of large area arrays of nanometric silicon tips, for use as Field Emission Devices (FEDs). The process combines Interference Lithography (IL) with isotropic Reactive Ion Etching (RIE). Si tips with typical curvature radius of 20 nm and height of 900 nm were recorded with a periodicity of 1 μm (density of 10^6 tips/mm^2) covering a Silicon wafer of 2 in. The measurement of the electrical performance of the arrays demonstrates the feasibility of the association of these two techniques for recording Field Emission Tips.

1. Introduction

Silicon tips are very interesting structures that can be used for fabrication of Field Emission Devices (FED) [1–4] such as Flat Panel Displays (FPD) [1–3], microwave power tubes [1,2], pressure sensors [1,2,5,6] and electron source for X-ray devices [7]. There are also other types of applications that are not based in electron emission as for example tips for scanning microscopy [8,9], MEMS [10,11], biomedical applications [12,13] or antireflection coatings on silicon [11,14].

For Field Emission applications the radius of curvature of the tip and the array density [1,15] are important parameters for determining the efficiency of the device. Thus the lithography is one of the most important features in the manufacturing of FEDs. The optical lithography is the simplest and less-expensive lithographic technique, but its low resolution limits the size of the tip as well as the density of the arrays. Although nowadays, deep UV steppers allow the lithography of structures up to 100 nm [16], such systems are very expensive or dedicated to certain processes in microelectronic industry. Focused Ion Beam (FIB) or E-beam systems are multipurpose equipments that achieved high resolution; however, the sequential nature of these recording processes requires long time to perform large areas, resulting also in high costs. Thus the Interference Lithography (IL) is a cheaper alternative to record submicrometric periodic patterns in large areas [17–19]. Although the IL has been already proposed [17] to record photoresist periodic patterns for manufacturing of Field Emission Tips, the complete manufacturing of the tip arrays using IL never has been demonstrated neither measured the emitting ability of the tips.

The problem for using IL is the low contrast of the sinusoidal fringe pattern that make difficult the recording of high aspect ratio photoresist structures. Besides this fact IL is not a usual process in the manufacturing of semiconductor devices. In addition, the use of high coherent light sources, required to create the interference patterns, increases very much the contrast of the Standing Waves (SW) [20,21] pattern generated by the reflection on the Si substrates, requiring the use of antireflection coatings (AR) [18,20,22,23].

In this paper we propose and demonstrate a few steps process, fully compatible with the Si technologies, that associates Interference Lithography and the isotropic RIE for recording Field Emission Silicon tips.

2. The tips fabrication process

In general, two types of process are used for the fabrication of tips arrays: the Spindt-type process and the Silicon tip-on post process. The Spindt-type process is used for fabrication of metallic tips by deposition or evaporation [1,2,24,25] and the Interference Lithography may be used to define the gate pattern. Many applications, however, require the fabrication of silicon tips for integration in microelectronics devices. Thus in the silicon tip-on-post type process [1,2,19], the etching of the silicon substrate forms the tips,

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in this case the Interference Lithography may be used to define the mask pattern for etching.

The proposed process is based in the silicon tip-on-post process [1,2,19] as schematized in Fig. 1 with the following steps: the thermal growing of a SiO_2 film, the Interference Lithography of photoresist structures, the patterning of the SiO_2 by RIE, and the etching of the Si by RIE to form the tips. As substrates were used <1 0 0> oriented n-type silicon wafers with resistivity 4.7 Ω cm cleaned by RCA standard procedures. On the substrate, a SiO_2 film was thermally growth with a thickness of 157.4 nm. After the oxidation, the wafer is coated with a positive photoresist Az1518 film of about 700 nm of thickness and pre-baked @70 °C during 20 min.

The fringe light pattern is generated by an interferometer using an Ar laser operating at the wavelength 457.9 nm as light source. The expanded beams interferes at the sample forming a circular spot with about 10 cm of diameter, that presents a wave-front quality of about λ/4. Such wave-front quality implies in a maximum distortion of the fringes of a quarter of period in same area. The fringe period is defined by the angle formed between the interfering beams [26], in our setup can be varied between 0.4 to 1.6 μm. To warrant high contrast patterns, our optical setup is provided with a Fringe-Locker system [27] that locks the interference fringes during the exposure.

The photoresist film is exposed twice to the same fringe pattern using a light energy dose of 380 mJ/cm^2, in each exposure. In order to achieve a two-dimensional pattern, the sample is rotated of 90° between the exposures. In this case, the samples were exposed to a fringe pattern with period $\Lambda = 1$ μm, that results in a Standing Wave (SW) pattern of period equal to 158 nm. In order to reduce the contrast of the SW it is possible to use BARC (Bottom Antireflective Coatings) [18,20,22,23], but the use of such coatings introduces more steps in the lithographic process. In a previous paper [21] we demonstrated that the use of a SiO_2 film with thickness equal to one complete SW period, instead the BARC, allows the recording of deep photoresist structures on Si substrates with over cut profile and without any residual photoresist on the SiO_2/Si substrate. Although the SiO_2 film does not eliminate the contrast of the SW pattern it improves the lithography [21] and has the advantage that SiO_2 is an excellent mask for high selective RIE etching of the silicon substrate.

After exposition and development of the photoresist using MIF 312 diluted 1:1 in deionized water, during 40 s, a square array of two-dimensional photoresist structures are obtained [21]. The Fig. 2 shows a SEM image of the holographic pattern recorded in photoresist. Due the double exposure of fringe periods of $\Lambda = 1$ μm, the recorded photoresist structures (Fig. 2a) are posts

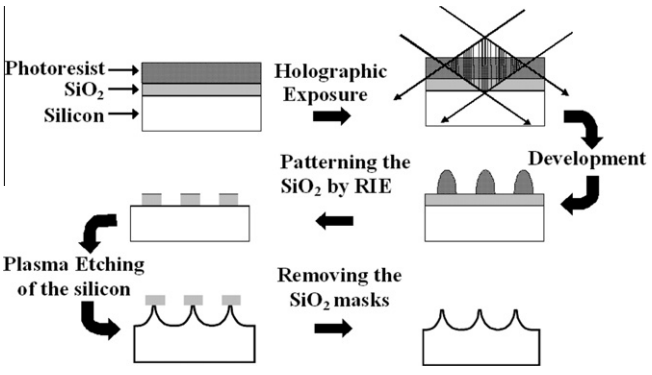

Fig. 1. Fabrication diagram of the silicon nano tips array. A SiO_2 film is thermally grown on the silicon wafer and then covered with a photoresist film that is exposure twice to the interference light pattern to record a two-dimensional array. The SiO_2 film is then patterned with a CF_4 plasma etching and the tips are formed by the etching of the silicon substrate in SF_6/O_2 plasma RIE.

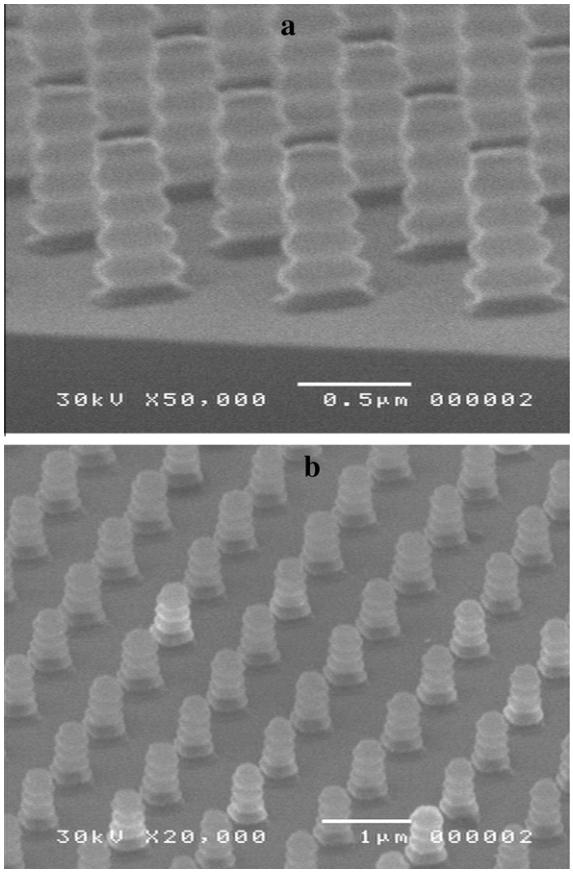

Fig. 2. SEM images of photoresist structures formed by Interference Lithography: (a) cross-section of high aspect ratio (2.3) structures and b) perspective view of the array with density of 10^6 structures/mm^2.

with ≈ 700 nm of height and mean diameter of ≈300 nm, arrangement in a square array density of 10^6 structures/mm^2. Note the presence of a well-defined ripple in the sidewalls of the structures caused by the SW pattern. Besides this ripple, high aspect ratio (depth/base ≈ 2.3) photoresist structures were lithographed in whole area of the silicon wafers with diameter of 2 in. Note also that the photoresist was completely removed among the recorded structures and the bottom of the SiO_2 interface is completely clear. This is a key point for the success of the process, because the obtaining of deep photoresist structures allows the direct patterning of the SiO_2 layer without use of any intermediate mask.

For the RIE steps it was used a homemade system [28], composed of a parallel plate reactor in which the discharge was sustained by a 13.56 MHz RF power, supplied to the lower electrode through an impedance-matching network.

The first RIE step is a CF_4 plasma etching of the SiO_2 that it transfers the photoresist pattern to the SiO_2. The used CF_4 gas flow was 100 sccm and the RF power was 50 W. After this step, the residual photoresist was removed using O_2 plasma etching. The Fig. 3 shows the patterned SiO_2 after the removal of the photoresist. Fig. 3a corresponds to a SEM image that shows the cross-section of the structures with a profile approximately cylindrical and average diameter of about 300 nm. The height of the structures is about 157 nm, which correspond to the initial thickness of the SiO_2 film. Fig. 3b is a low magnification microscopy of a top view of the array of cylindrical SiO_2 structures.

To form the silicon tips, was employed a RIE plasma with a mixture of SF_6 and O_2 gases using the patterned SiO_2 as a mask. In this gas mixture, the O_2 function is change the isotropy of the etching

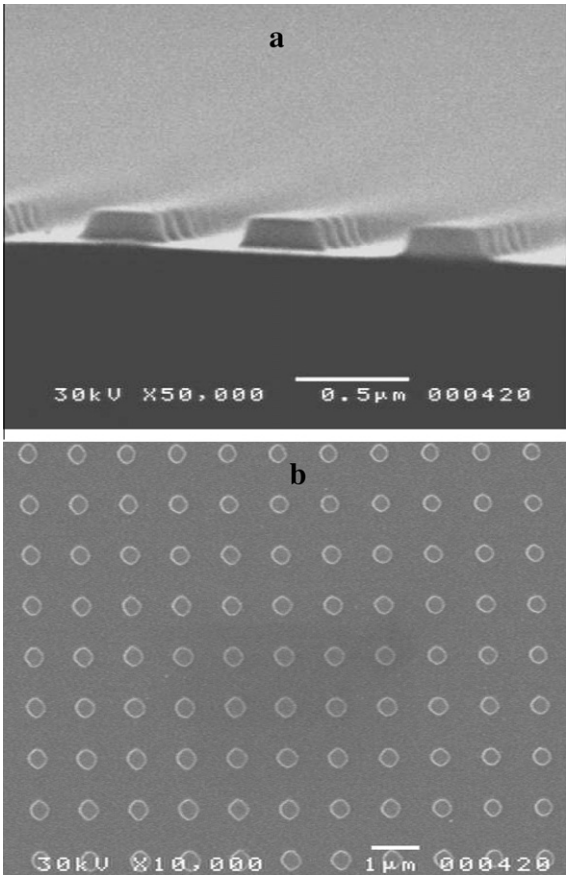

Fig. 3. SEM images of the patterned SiO_2: (a) cross-section of the SiO_2 posts and (b) top view of the patterned SiO_2 film.

[29]. Consequently, different shapes of the tips can be obtained changing the ratio SF_6/O_2. In particular, we perform the RIE using two different mixtures: a pure SF_6 gas with flow of 30 sccm and a mixture of SF_6:O_2 in the ratio 3:1 but keeping a SF_6 flow of 30 sccm and O_2 flow of 10 sccm. In booths cases was applied a RF power of 50 W. After the dry etching of the silicon, the SiO_2 masks were removed by wet etching in a buffered HF solution.

The first Si etching using a RIE with pure SF_6 results in tips with height of about 570 nm and diameter of about 120 nm on the top of the tip, as shown in Fig. 4. These tips are sharper near to half of their height, due to the isotropy of the pure SF_6 plasma etching. Such profiles are not appropriate because they cause breakdown of the tips (Fig. 4).

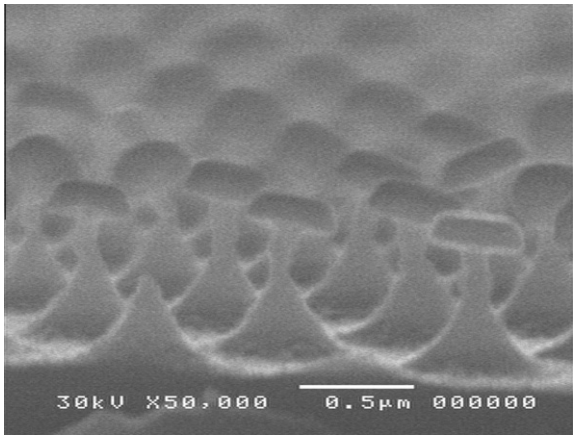

Fig. 4. Cross-section view of the tips obtained by etching of the silicon in pure SF_6 RIE.

Using the RIE with a mixture of SF_6/O_2, with the ratio of 3:1, tips with of about 900 nm of high and top diameters of 60 nm were obtained. The SEM images of the samples are shown in Fig. 5a, yet with the SiO_2 mask on the top of the tip. Controlling the time of the silicon RIE we can reach the minimum tip diameter able to sustaining the SiO_2 masks. Thus, using such process conditions, the sharpest fabricated tip presents a curvature radius of about 20 nm (on the top) and height of about 1 µm. The SEM image of these tips is shown in Fig. 5b that shows a perspective view of the squared array of the nanotips with density of 10^6 tips/mm^2. Note also that, the addition of O_2 allows the fabrication of nano tips sharper in the top [29].

Notice from Figs. 4 and 5a that, due the high selectivity of the SF_6 plasma etching, the SiO_2 mask remains intact after the silicon etching. Thus, this process give possibility which, before the removal of the SiO_2 masks, self-alignment steps can be introduced to deposit an insulator material between the tips as well as to integrate the gate electrode [1,2].

3. Electrical performance

The fabricated high-density array of silicon nanotips, showed in the Fig. 5b, was operated as a field electron emission device for the characterization of the current–voltage dependence and the temporal stability of the electron current.

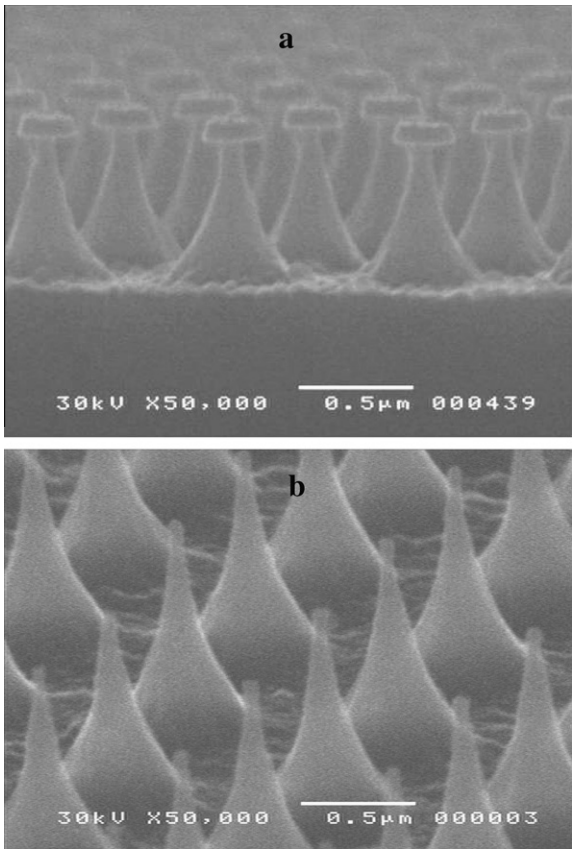

Fig. 5. SEM images of the silicon tips obtained by the etching of the silicon by SF_6/O_2 (3:1) RIE: (a) cross-section view of the tips yet with the SiO_2 masks on the top, b) view of the sharpest tips fabricated after the SiO_2 removal in a buffered HF solution. The tips have height of about 1 µm and curvature radius of about 20 nm which form an array with density of 10^6 tips/mm^2 recorded homogenously in a wafer of 2 in. of diameter.

Structures with small radius of curvature, as the tips, induce the concentration of the electric field lines that produces an intense field around the tip. If a voltage V_g is applied between the tip and the anode, which are distanced of τ, the electric field around the tip is given by:

$$E = \frac{\gamma V_g}{\tau} \tag{1}$$

where γ is called field enhanced factor of the tip.

The electron emission–current (I_e) by field effect in a silicon tip is described by the Fowler Nordheim (FN) tunneling theory [9], and its emission current can be modeled as:

$$\frac{I_e}{V_g^2} = A \exp\left[-B/V_g\right] \tag{2}$$

The A and B are known as FN parameters and are given by:

$$\begin{aligned} A &= 1.5 \times 10^{-6} \exp\left[10.4/\Phi^{1/2}\right] \frac{\alpha\gamma^2}{\Phi\tau^2} \\ B &= 6.44 \times 10^7 \Phi^{3/2} \frac{\tau}{\gamma} \end{aligned} \tag{3}$$

where Φ is the tip material work function and α the emission area.

Eq. (2) can be also re-writing as a linear relation that is known as Fowler Nordheim equation:

$$\ln\left[\frac{I_e}{V_g^2}\right] = \frac{-B}{V_g} + \ln(A) \tag{4}$$

Fig. 6 shows a diagram of the measurement system for $I_e \times V_g$ characteristics. The silicon nanotips array was placed inside a vacuum chamber (residual gas pressure below 10^{-7} mbar) and connected on a Cu cathode using silver paint as a conductive adhesive layer. The 1.5 mm diameter stainless steel anode was polished to mirror quality and placed on a micrometer head that allows the controller of the distance between the silicon nanotips and the anode. The data acquisition is fully automated; the computer communicates with a Keithley voltage supply (HVS model 248) and the electrometer (SE model 6514), acquiring the $I_e \times V_g$ data points. Assuming a fixed distance tip/anode τ = 50 μm, the anode voltage was scanned from 0 to 1.5 kV in steps of 50 V. Fig. 7a shows the experimental points, where each point plotted represents the average of 20 current readings. The electron emission starts (I_e > 1 μA) when a voltage $V_g^{threshold} = 900$ V is applied. If the voltage V_g = 1500 V is applied the measured current was $I_e \approx 50$ μA. In order to obtain the FN parameters, the experimental data points are plotted in the FN form (Eq. (4)) as shown in Fig. 7b. Note that the experimental data points are in agreement with FN equation (Eq. (4)) that make possible realize a linear fit of these points and obtain the linear (ln(A)) and the angular (B) coefficients, that assume the values: ln(A) = −19.54 e and B = 7320 V. Replacing the FN parameters values in Eq. (2), can be estimated the response of the measured nanotips array for different tip/anode distance. These estimated $I_e \times V_g$ curves are showed in Fig. 8 together with the experimental data points. For the tip/anode distance τ = 40 μm the threshold voltage is reduced to $V_g^{threshold} = 710$ V and due the exponential dependence between the current and the applied voltage (Eq. (2)), the electron current to V_g = 1500 V is increased to $I_e \approx 0.25$ mA. For τ = 40 μm the threshold voltage is about 570 V and the electron current to V_g = 1500 V is $I_e \approx 0.7$ mA.

The temporal stability of the emitted current was also measured. In this way, a voltage V_g = 1500 V was applied during 5 h 30 min, Fig. 9 shows the measured $I_e(V_g = 1500\ \text{V}) \times$ time curve. For the initial 2 h the current present expressive variations. After this period, the electron emission current present a stability behavior, the current assume the value I_e = 53 μA and the variations are

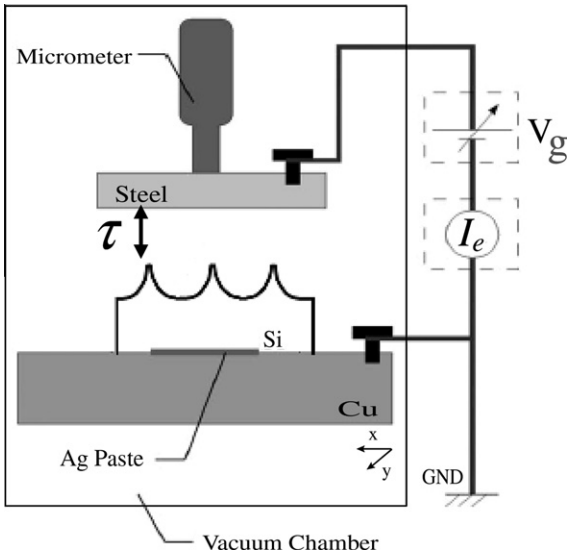

Fig. 6. Schematic description of the setup for the electrical characterization of the silicon nanotips array. A voltage V_g is applied between the tips and Cu anode; the electron emitted current I_e is measured by the electrometer.

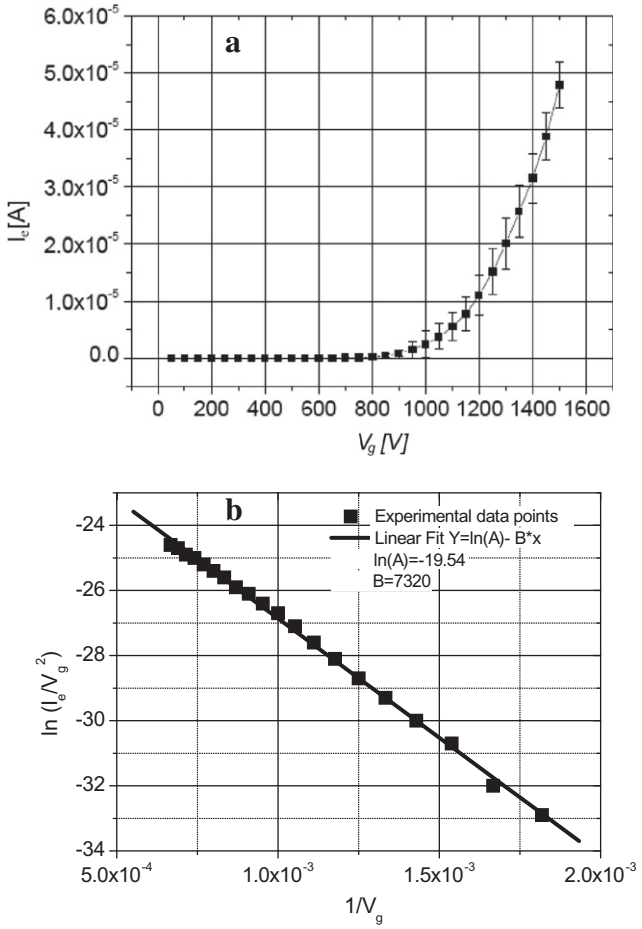

Fig. 7. (a) Characteristic $I_e \times V_g$ curve of the nanotips array showed in Fig. 5(b) measured for a tip/anode distance τ = 50 μm. The electron emission starts when a voltage $V_g^{threshold} = 900$ V is applied, when the voltage reach V_g = 1500 V was measured a current $I_e \approx 50$ μA. (b) the experimental data point plotted in the FN form in order to fit this points and obtain the FN parameters.

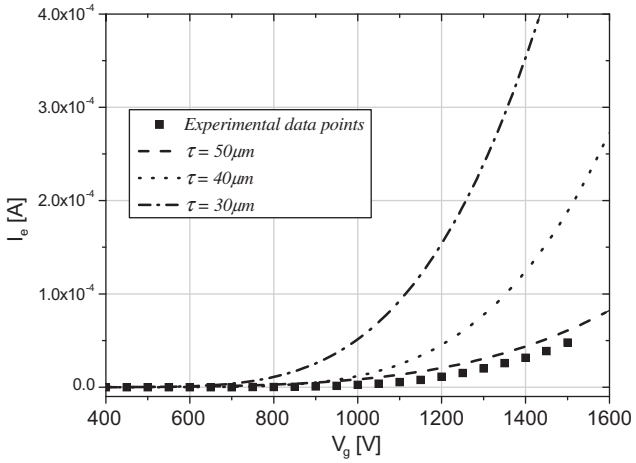

Fig. 8. $I_e \times V_g$ curves, experimental and estimated curves for different tip/anode distances.

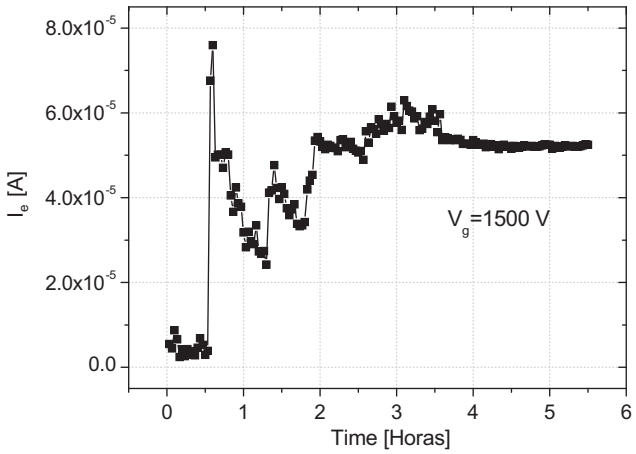

Fig. 9. Temporal stability curve measured for the silicon nanotips array showed in the Fig. 5b. After an initial instability, that can be associated with the presence of silicon dioxide or chemisorptions at the tip surface, the current assume an establish value.

smaller than 4% of this value. About the initial instability, there are some papers that relate this phenomenon with two mechanisms: the presence of silicon oxide over the tip surface and the chemisorptions of residual gases. Both mechanisms can modify the surface work function [1,28,30].

4. Conclusions

We demonstrated a simple and low cost process for manufacturing of Field Emission Si tips using Interference Lithography and isotropic Reactive Ion Etching. In particular, the use of proper thickness of SiO_2 avoids the use of BARC as well as it can be used as a selective mask for etching the Si, reducing the steps of the RIE and using materials fully compatible with the silicon technologies. The obtained silicon tips have curvature radius of about 20 nm on the top and height of about 1 μm, distributed in a square array with density of 10^6 tips/mm^2 covering an area of about 3 in.^{2}. Using a smaller wavelength laser in the interferometer, densities up to 10^7 tips/mm^2 can be achieved.

The FED was characterized by measurement of the current–voltage and temporal stability curves. The emission current for a tip/anode distance of 50 μm, start when $V_g^{threshold} = 900$ V, while for $V_g = 1500$ V the measured current was $I_e \approx 50$ μA. The current–voltage curve is in agreement with the Fowler–Nordheim tunneling model that allows estimating the performance of this device for another tip/anode distances. Thus, for the distance tip/anode of 30 μm was calculated the threshold voltage $V_g^{threshold} = 570$ V and the current for $V_g = 1500$ V was around $I_e \approx 0.7$ mA. The temporal stability of the electron emitted current show that after a initial current instability the current remains stead with variations smaller than 4% of the current value that is $I_e = 53$ μA.

The measured electrical performance of the arrays demonstrates that the use of IL is a process compatible with the VLSI technologies. For the next developments a gate electrode can be integrated to this tips array using the SiO_2 masks as a self-alignment way.

Acknowledgments

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